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DEVELOPMENT OF LONG WAVELENGTH SINGLE LONGITUDINAL (SLM) INJECT-ETC(1)

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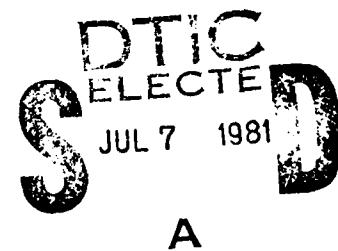
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
MERADCOM - DAAK 70-79-C-0239

DEVELOPMENT OF LONG WAVELENGTH SINGLE
LONGITUDINAL MODE (SLM) INJECTION LASER DIODES

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FINAL TECHNICAL REPORT
DECEMBER 30, 1980

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- i. Optimization of the double heterojunction DH structure.
- ii. Process development connected with the fabrication of buried heterojunction BH laser structures.
- iii. Modification BH laser structure and fabrication technique to optimize severe melt back.
- iv. Modification of the regrowth LPE technique to resolve melt back and the optimization of the N-P reverse bias junctions.
- v. Device performance.

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1.0

INTRODUCTION

The primary objective of this program was the development of a single longitudinal mode (SLM) injection laser source in the 1.0 to 1.3 micron wavelength region. More specifically, the initial design described in the technical approach consists of a buried-heterostructure BH double heterostructure waveguide optical cavity formed in a two step liquid phase epitaxial (LPE) synthesis. The initial design is similar to that described by Hitachi Ltd. at the 37th Annual Device Research Conference (June 79, Boulder, Colorado).

This report describes efforts directed toward the optimization of fabricating (SLM) injection sources and will concentrate on the following topics:

- a) Materials and structure development required to produce longwavelength SLM injection diodes.
- b) Process development required for the fabrication of BH laser diodes.
- c) Optimization of the BH laser structure.
- d) Device performance including threshold, DQE, and wavelength optimization.

2.0 BACKGROUND

DH GaInAsP/InP diode lasers with emission wavelengths in the 1.0 to 1.3 micron range are considered to be most promising light sources for long distance, high bit rate, optical fiber communication systems. The dispersion in silica materials vanishes at 1.27 microns and the total dispersion, including waveguide dispersion, can be reduced to the 1.3 - 1.6 microns wavelength range. This also provides a better spectral match to the fiber optic waveguide transmission window.

3.0 MATERIALS AND STRUCTURE DEVELOPMENT

3.1 GaInAsP DH Structure

During the first quarter, all the work was aimed at optimizing the GaInAsP/InP laser structure to be utilized in the development of the buried heterojunction lasers. The DH structure is the first part of a two step LPE technique. This structure is shown in Figure 1 and the layer construction is as follows:

Sn-doped InP substrate ($N \sim 2 \times 10^{18} \text{ cm}^{-3}$) with $<100>$ orientation with an etch pit density (EPD) of $<7 \times 10^4 / \text{cm}^2$;
Sn doped N-InP cladding layer ($N \sim 1 \times 10^{17} \text{ cm}^{-3}$); undoped N-In_{0.708}Ga_{0.292}As_{0.560}P_{0.440} quaternary active region ($N \sim 7.5 \times 10^{18} \text{ cm}^{-3}$); Zn doped InP cladding layer

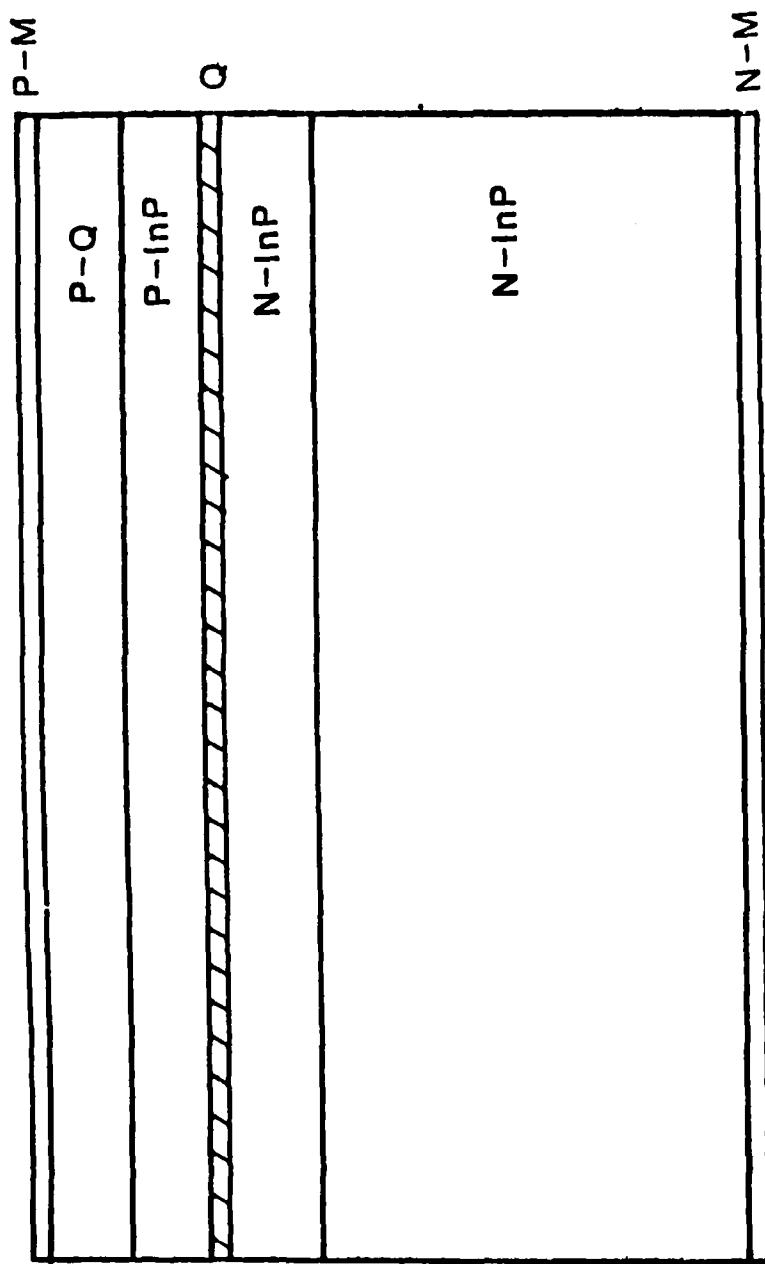


Figure 1 Four layer GaInAsP/InP DH Structure

($P \sim 1 \times 10^{18} \text{ cm}^{-3}$); and a Zn doped P-In_{0.802}Ga_{0.198}As_{0.445}P_{0.555} quaternary cap layer ($P \sim 2 \times 10^{18} \text{ cm}^{-3}$). Layer thicknesses are ~ 3.0 , 0.2-0.3, 7.5 and 0.65 μm respectively. Melt compositions for this type structure are summarized in Figure 2. Scanning Electron microphotographs (S.E.M.) shown in Figure 3, show a stained cross section of the quaternary used in the fabrication of the DH laser structure. The three S.E.M. photographs in Figure 3a, b, c, are taken from the lead, center and trailing regions of the EPI wafer respectively. Uniformity of the layers is excellent for the GaInAsP/InP material system. Figure 4 outlines the actual dimensions for each of the sampling points. Taper in the active region (2) is approximately 16% across the surface of the EPI wafer; whereas, the thicker layers (3,4) show approximately 8% and 14% taper respectively. Figure 3b also shows an EBIC (Electron Beam Induced Current) trace super-imposed on the EPI layer micrograph. The diffused P/N junction is not visible within the action region since the particular etch used to delineate layer interfaces is not sensitive to doping type. The trace, however, clearly shows the location of the P/N junction centered within the quaternary active layer.

INP - LPE REI SHEET

Run # RO-159

Crystal # InP434-R4

Furnace/Boat Al/RD3-A

date 9/15/9-16-80

Slice/Thickness #14-C/10.0

Operator D.L.

A.10 MTorr

A. 400cc
Flow Rate:

A. 45 min

A. 180 min.

Temp: 644.5°C

Rate: $8^{\circ}\text{C}/\text{hr}$

Grow: 636.0°C

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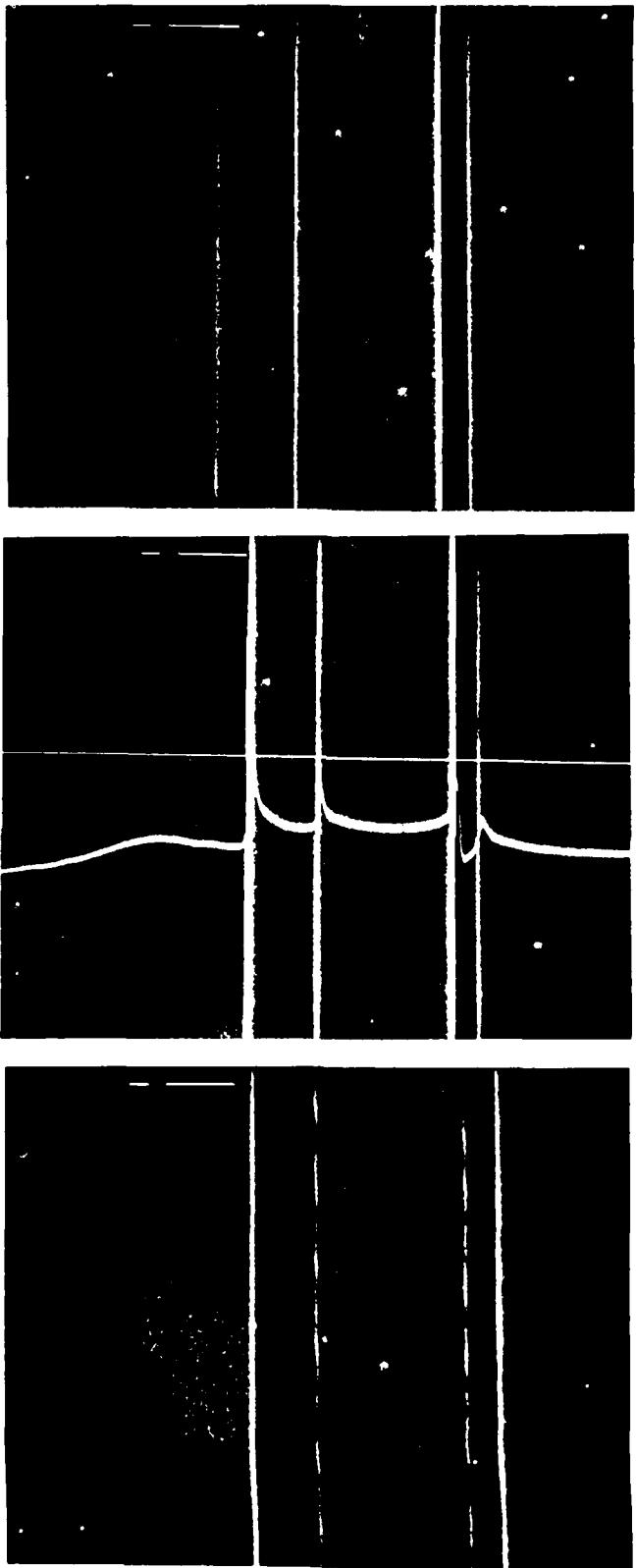
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4 layer structure

Figure 2 Melt composition of four layer structure

(10Kx)



a. Lead
b. Center
w/EBIC Scan
c. Trail

Figure 3 SEM microphotographs with (EBIC) 10Kx

REQUISITION FOR SEM MICROGRAPH

Sample # QBH 186 Date: 10/12/80

Structure:

Type of Micrograph Required: SE AE/EBIC-LS Magnification

Thickness: SE _____

LAYER	LEFT	CENTER	RIGHT	AVERAGE
1. InP (Clad)	-	-	-	3
2. Q(Active)	0.13	0.17	0.22	0.17
3. InP (Clad)	2.32	2.17	2.11	2.20
4. Q (Cap)	1.00	1.19	1.17	1.12
5.				
6.				
7.				
8.				

REMARKS: Etched in 6:1:1:, H₂SO₄: H₂O₂: H₂O for 50 seconds to delineate junctions.

Figure 4 Layer thickness of GainAsP/InP (DH) structure

P/N junction is indicated by the EBIC in Layer 2).

In order to properly interpret S.E.M. photograph shown in Figure 3b, the EBIC scan direction is from top to bottom. The induced current waveform will move in the right direction, designating an N-type junction or N to P type conversation. The induced current waveform moving to the left designates a P-type or a P to N type conversion. As can be seen in this photograph the leading P-N junction is well defined by the EBIC scan.

3.2 OPTIMIZATION

Using this structure the prime considerations that had to be optimized were the LPE growth parameters to insure the following:

- A. Layer thickness control;
- B. P/N Junction location in the active region;
- C. Wavelength control vs. growth parameter.

A. Layer thickness control was accomplished and is shown in Figure 3. This was accomplished by using the appropriate melts consisting of pure Indium and dopants amounts of InP, InAs, and GaAs. These melts were then saturated at 645° for 3 hours. The boat containing the melt compositions was then cooled to room temperature and removed from the EPI system. The InP substrate and N/P dopants were then added to the EPI boat and re-saturated for 1.5 hours at 645°C before growth was initiated. This eliminated the severe thermal etching of the InP substrate during the saturation period. Growth was started at 635°C using a 5 second pure In etch melt. Using a cooling rate of 0.8°C/Min during the growth cycle produced a controllable layer thickness as well as excellent surface morphology.

B. Since the zinc diffusion co-efficient of InP at a growth temperature of 635°C is quite high (estimated to be around $10^{-11} \text{cm}^{-3} \text{sec}^{-1}$), zinc which is used as a P-type dopant will diffuse into the 2 adjacent layers during LPE growth.

C. Wavelength control which is of utmost importance was found to be controllable by using the chart shown in Figure 5. By using the proper amounts of GaAs and InAs for lattice matching the wavelength can be controlled to an error of less than 200^o A, Ref. 12.

Once the (DH) structure was optimized, meaning that layer thickness and wavelength was brought under control, the next steps undertaken were to develop a technique suitable to fabricate buried heterojunction laser structures to produce (SLM) single longitudinal mode injection lasers. This includes all techniques involved such as etching techniques to form reverse mesa structure using the DH structure previously explained, and also a suitable LPE technique to regrow the N-P reverse bias junction confining the etched mesa structure. These techniques and others will be explained herein.

4.0 FABRICATION TECHNIQUES OF BURIED HETEROJUNCTION LASER STRUCTURES

4.1 A standard GaInAsP/InP (DH) structure which was explained previously and shown in Figure 1, is used in order to generate buried heterojunction structures.

Figure 6a-i - shows the fabrication techniques step by step. The standard GaInAsP/InP structure is shown after LPE, in Figure 6a.

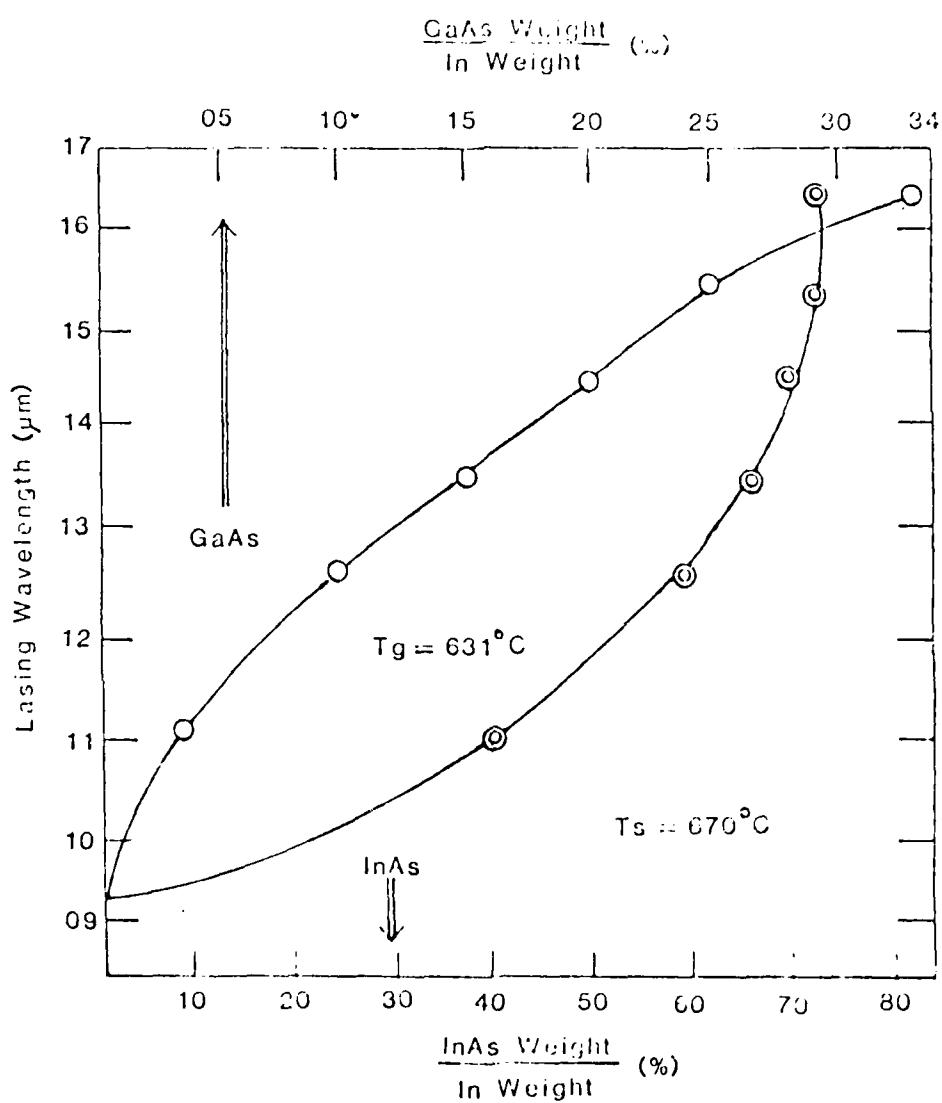


Figure 5 Dependence of lasing wavelength on liquidus composition for lattice matched GaInAsP

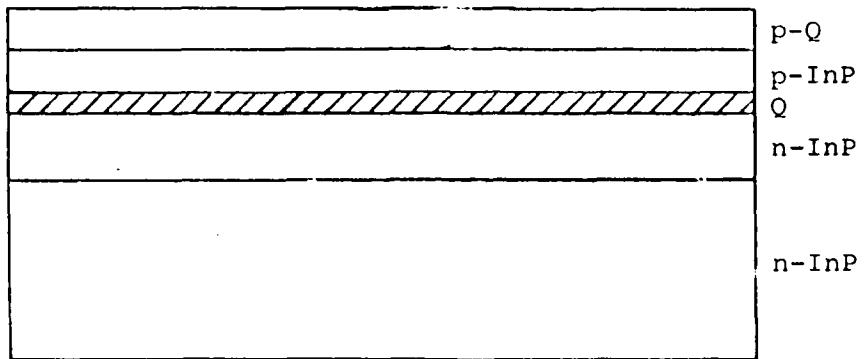


Figure 6a. GaInAsP/InP DH Structure

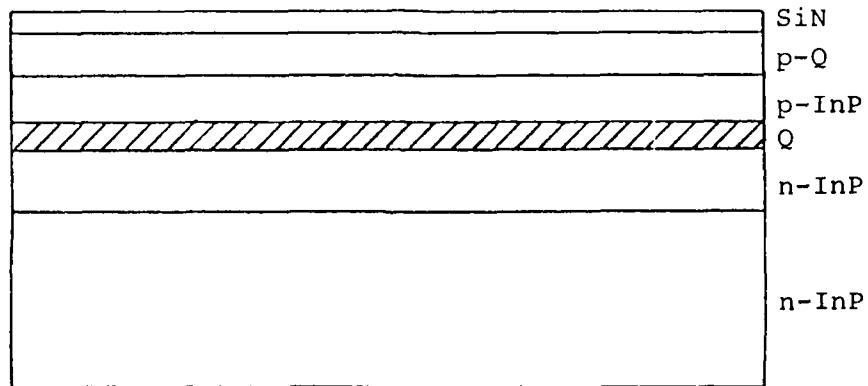


Figure 6b. Deposit Nitride

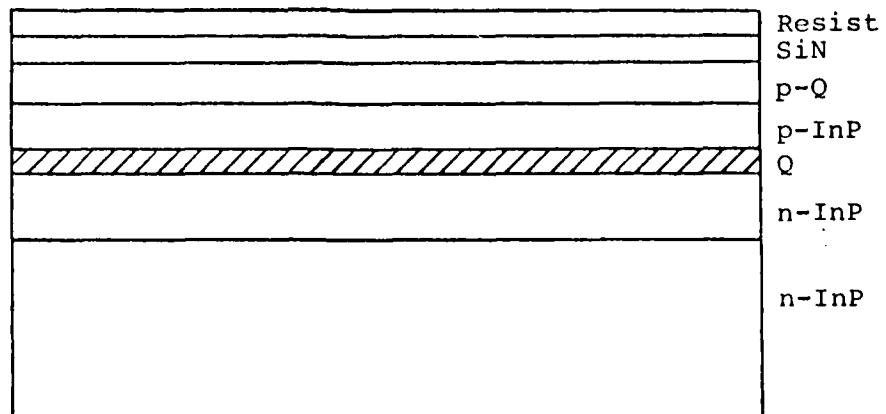


Figure 6c. Photoresist

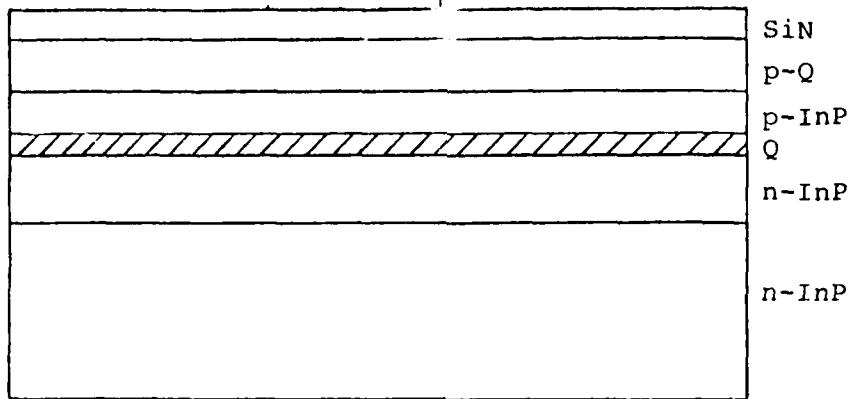


Figure 6d. Expose and Strip Resist

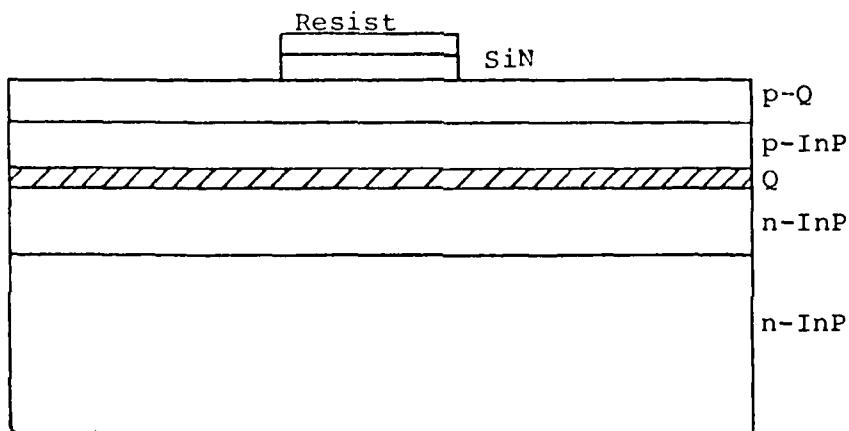


Figure 6e. Etch Nitride

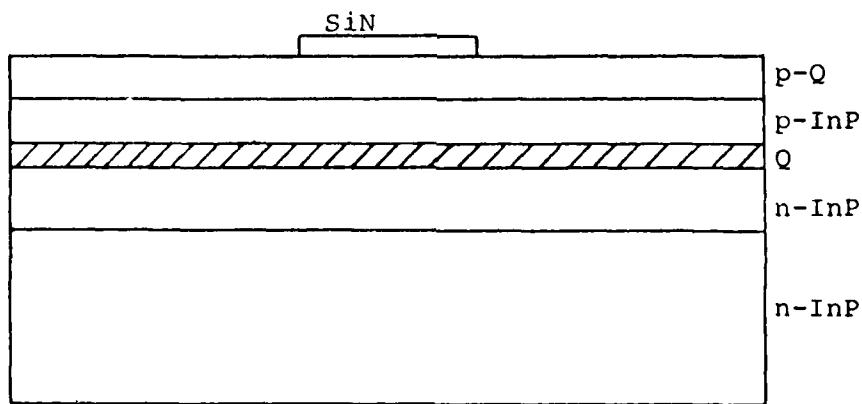


Figure 6f. Strip Resist

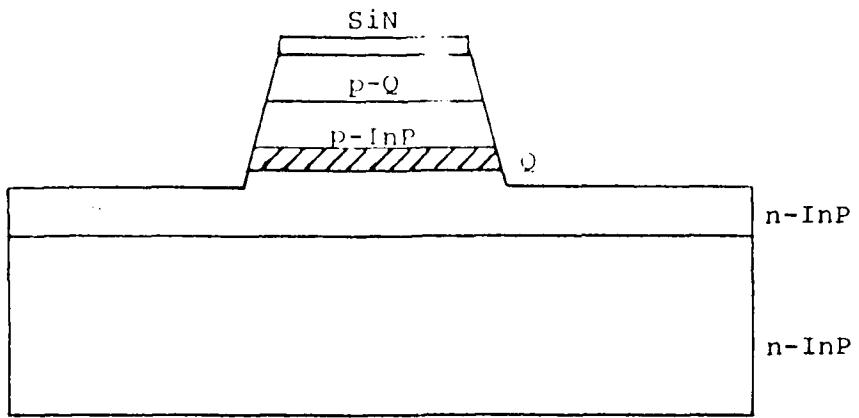


Figure 6g. Etch DH Structure to Form Mesa

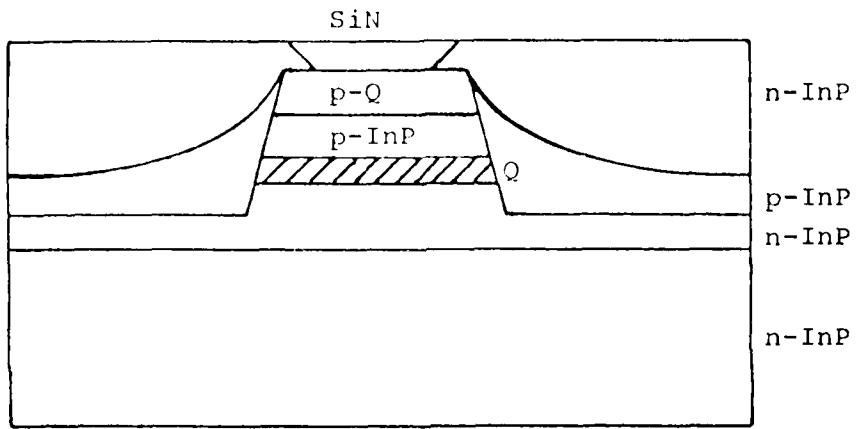


Figure 6h. Regrow LPE layers to Form Buried Heterostructure

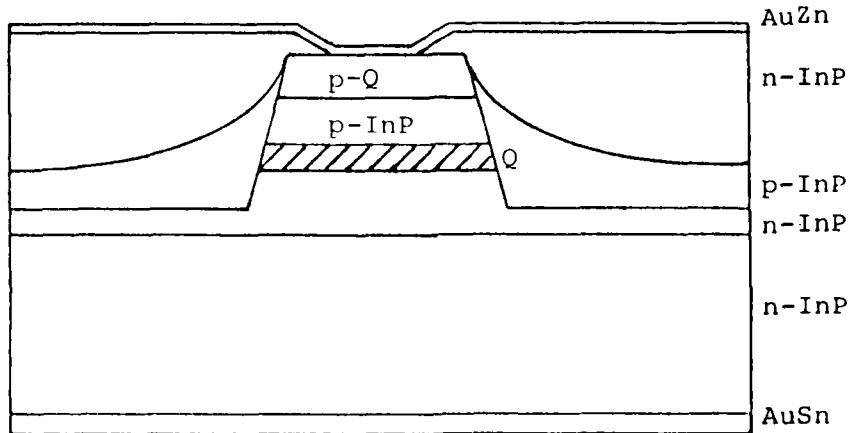


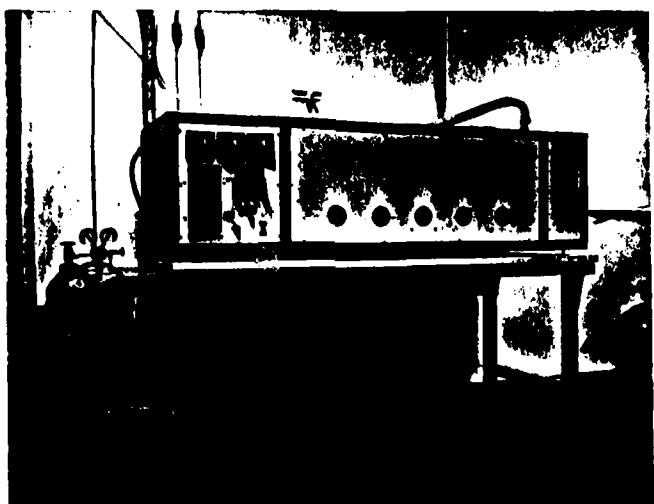
Figure 6i. Remove Nitride and Metallize Wafer

4.2 CHEMICAL VAPOR DEPOSITION (CVD)

To form the stripe geometry mask for etching mesa stripes, a silicon nitride (Si_3N_4) layer 800 \AA thick must be deposited onto the GaInAsP/InP epitaxial wafer shown in Figures 6b. The CVD system, shown in Figure 7 has the capability of depositing both silicon nitride (Si_3N_4) and silicon oxide (SiO_2) films. These films are deposited at 600 $^{\circ}\text{C}$ by a gaseous reaction of silane (SiH_4), ammonia (NH_3), and oxygen (O_2) by direct thermal activation in a nitrogen (N_2) carrier gas.

In the deposition of a silicon nitride film, mixtures of (SiH_4) and (NH_3) are thermally decomposed using an (N_2) carrier gas at 600 $^{\circ}\text{C}$. A SiH_4/NH_3 ratio of 1:5 results in a deposition rate of $\sim 40\text{\AA}/\text{min}$.

Figure 8 shows a gas schematic of the CVD system. The system provides for an extremely controllable and reproducible process not only for GaInAsP/InP production, but also in other standard products, such as GaAlAs etched well L.E.D.'s and single mode (CSP) laser structures.



**Fig. 7 (CVD) Chemical Vapor Deposition
System, for both SiO_2 and Si_3N_4**

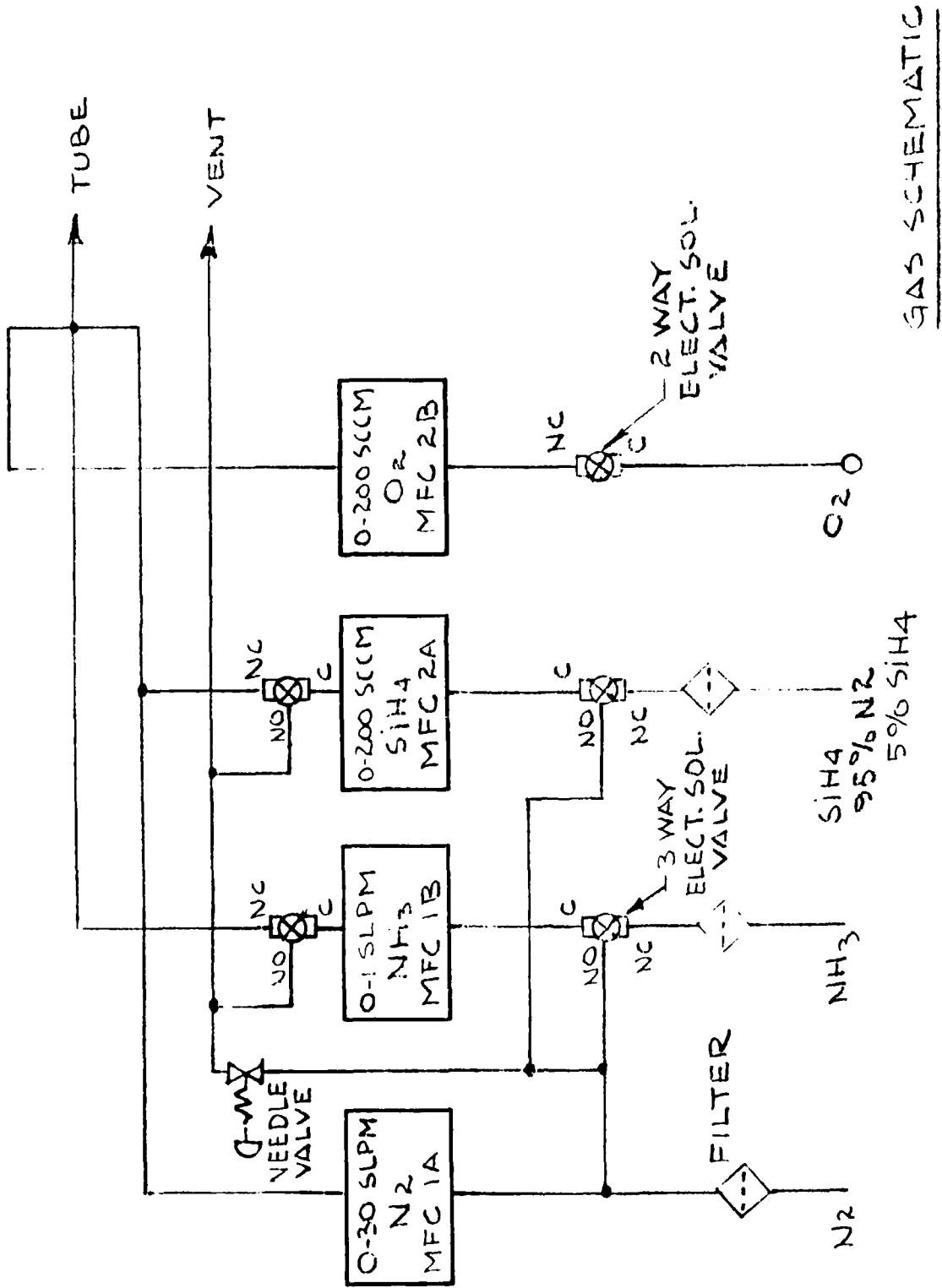


Fig. 8 (CVD) gas schematic

4.3

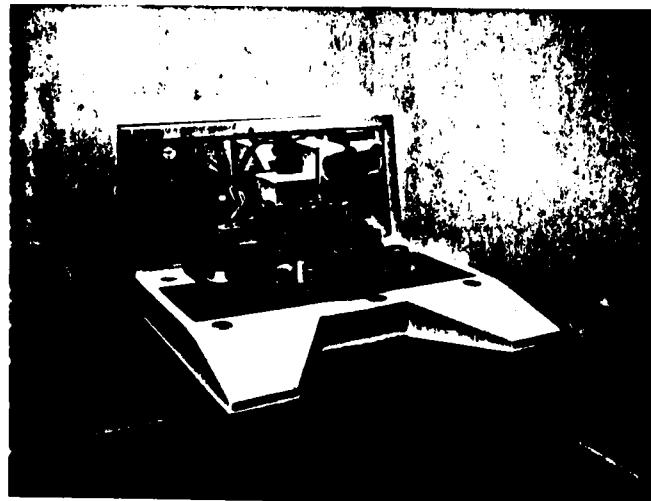
PHOTOLITHOGRAPHY

The method used to form stripe geometry patterns Figure 6c, on GaInAsP is a standard photolithographic technique also used for processing GaAlAs LED's and CW laser diodes.

In this procedure, positive photo resist (Hunt Chemical Corp. HPR204) is applied to the GaInAsP/InP wafer using a spinner. The resist is spun-on at 4,000 RPM for 40 seconds, yielding a film thickness of 5,000 Å. The coated wafer is then baked for 20 Min. at 120 °C. The pre-bake cycle prepared the photo resist for exposure to ultra-violet light by removing solvents from the coating, making it more sensitive to the UV.

Alignment and exposure is performed using a Kulicke and Soffa high speed mask aligner and exposure system shown in Figure 9.

The developing of the exposed wafer is done using Hunt Corp. I.S.I. developer. A post bake (120 °C) anneals the resist and prepared the wafer for plasma etching, to open the diffusion windows through the Si_3N_4 mask. The mask size used as a diffusion window is 5 μm wide. The steps described here are shown in Figures 6c thru 6d.



**Fig. 9 K&S exposure and alignment system
used to develop stripe geometry patterns**

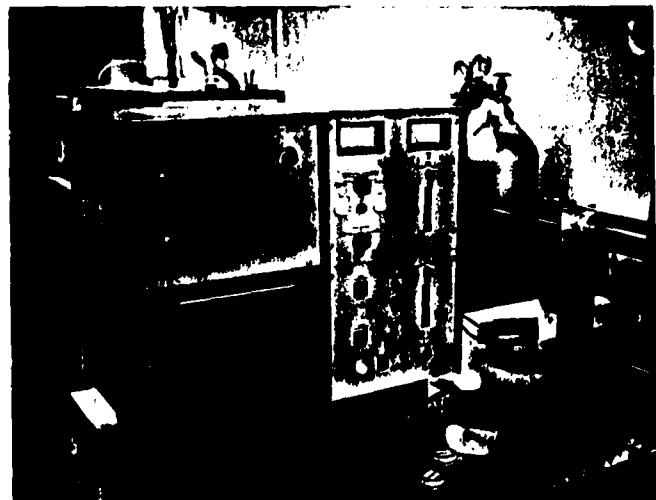
4.4 PLASMA ETCHING

To form the 10 μm Si_3N_4 stripes a LFE Corp. plasma asher (Model #PD5-302) is employed and shown in Figure 10.

The processed InGaAsP/InP structure is placed into the quartz slice boat in a vertical position and loaded into the Asher's reaction chamber. The chamber is maintained at an atmospheric pressure of 1.0 Torr. The gas mixture enters the reactor chamber at 50 cc/min. and is ignited by an RF power of 200 watts, at a temperature of 175 $^{\circ}\text{C}$. The Si_3N_4 film is selectively etched for 2 minutes at a rate of 425 $\text{\AA}/\text{Min}$. Once the cycle is completed, the wafer is removed and the photo mask stripped leaving a Si_3N_4 masked GaInAsP/InP wafer, ready for selective mesa etching Figure 6f.

CHEMICAL ETCHING

4.5 Mesa nitride which is shown in Figure 6G is used as an etching mask and later as a selective growth mask. Mesas are formed on the $<110>$ orientation by etching through the P-GaInAsP Active Region to the InP substrate, using bromine methanol (2% Br by volume). A subsequent LPE growth is performed using the Si_3N_4



**Fig. 10 (LFE) Plasma Etching System used to
etch selective patterns into Si_3N_4**

film as a growth mask resulting in the formation of reverse-biased junctions on either side of the mesa structure. This second LPE growth consists of a pure In melt (used as a melt back etch to remove defects and contaminants followed by a P-InP layer doped to $5 \times 10^{17} \text{ cm}^{-3}$ and an N-InP layer doped to $1 \times 10^{17} \text{ cm}^{-3}$ as shown in Figure 6h. Finally, the Si_3N_4 growth mask is removed.

4.6

AuZn, AuSn CONTRACT METALLIZATION

The processed wafer is back lapped to 3.5 mils, cleaned in organic solvents and rinsed in alcohol. Once the wafer is cleaned, it is loaded into the vacuum deposition system which is then evacuated to less than 10^{-6} Torr; the slice is heat treated to 250°C for 10 min. in order to drive off any remaining surface contamination. Metal evaporation is carried out, depositing 2000\AA of AuSn (95% Au, 5% Sn) on the n-side. This step is repeated on the p-side of the wafer using AuZn (95% Au, 5% Zn) deposited in two steps. First, a 500\AA layer is deposited serving as a heavily zinc doped interface which prevents any out diffusion of In during the evaporation of P-contacts. A second layer 1500\AA is subsequently deposited and the wafer removed from the vacuum system. The contacts are heat treated at

340 °C in H₂ for 60 seconds to anneal the ohmic contacts on both n-and p- sides. This is shown in Figure 6i.

Due to the complex fabrication requiring a two-step crystal growth, many different parameters had to be optimized: (A) Etching techniques to form the reverse trapezoidal pattern formed on the <110> crystal orientation. (B) Controlling the etch melt to minimize thermal etching of the trapezoidal mesa during growth. (C) Thickness control must be optimized in order to fill the area between adjacent mesa structures with both the P and N InP layers.

4.7

OPTIMIZATION

A. To successfully etch the (DH) GaInAsP/InP the following etches were investigated: HCl, H₃PO₄, 1:1; Acetic Acid, H₂O₂ H₂O (DI), 1:2:1; and bromine methanol 2% by volume. The graph showing time vs. depth is shown in Figure 11 for etching InP. All etches were used at room temperature and standard photolithographic techniques were applied to form the stripe geometry patterns, alignment was done in the <111> direction. Etch times in these experiments were 10, 15, 20 and 30 seconds for all the above mentioned etches.

Examples of InP substrate etching are shown in Figure 12 a, b and c with etch rates as follows: 0.08, 0.06 and 0.20 $\mu\text{m/sec}$, respectively. It was determined that the bromine methanol 2% by volume was the best of the 3 etches which produced a minimal amount of undercutting of photo resist mask.

It was also found that in order to regrow the reverse bias junction over the etched mesa, that the mesa structure had to be etched with $\langle 110 \rangle$ crystal orientation side walls. Using the $\langle 111 \rangle$ crystal orientation side wall resulted in poor nucleation of the regrown epitaxial reverse bias junction.

B. One of the major problems which hampered the success of the contract was minimizing the amount of melt back to the reverse trapezoid mesa during the regrowth of the reverse bias N-P junctions. In the first attempts regrowth was done using no etch melt. This was successful as far as not melting back the mesa structure, but resulted in poor nucleation of the regrowth. It was found

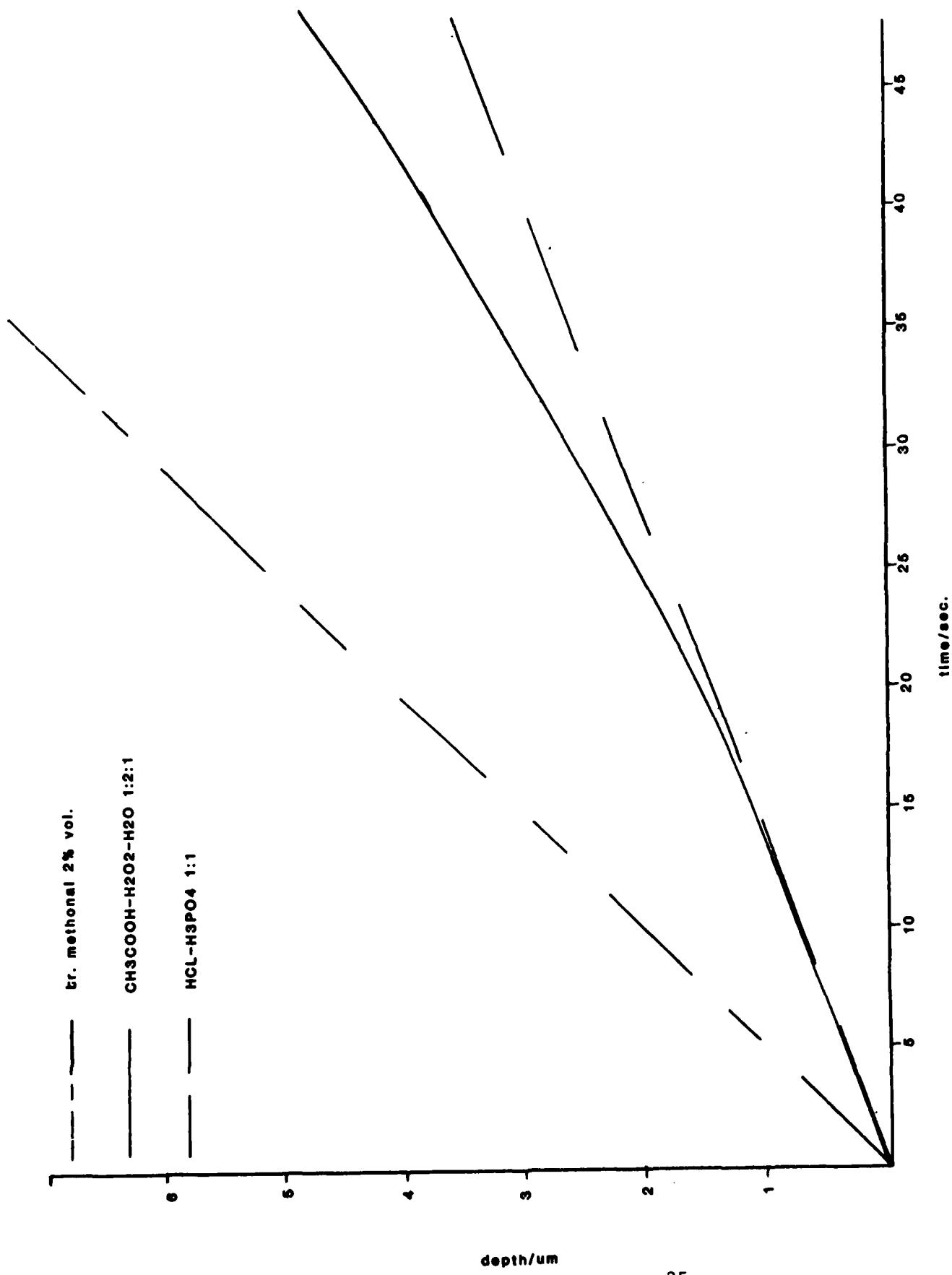


Figure 11 depth vs time



HCL-H₃PO₄ 1:1

30 seconds depth 2.5um



CH₃COOH-H₂O₂-H₂O 1:2:1

30 seconds depth 2um



Br. Methonal 2% / volume

30 seconds depth 6.5 um

Figure 12

that in order to initiate the epitaxial growth, an etch melt was needed in order to remove any contaminants and prepare the surface for the epitaxial layers; In using the pure (In) etch melt for five seconds, it was found that the mesa structure, mainly the P-GaInAsP cap layer would be reduced in size even with the aid of the Si_3N_4 regrowth mask over this layer. An example of this is shown in Figure 13a, b; Figure 14a, b - these are S.E.M. photographs of two completed epitaxial runs before and after regrowth; Figure 13 shows a photograph depicting an etched mesa structure before regrowth. Figure 13a, b shows mesa structure with cap layers $\sim 6\mu\text{m}$ wide narrowing to an active region of $\sim 4.5\mu\text{m}$ width. Figure 14a & b shows the structure after the regrowth of the (N-P) reverse bias junction. This shows that the P-GaInAsP cap layer was reduced to $\sim 1.2\mu\text{m}$ in width and the active region was reduced to $\sim 4.0\mu\text{m}$ in width. The main cause of the melt back is due to the etch melt. It was first thought that the Si_3N_4 mask was too thick and was introducing stress and causing the excessive melt back to the cap layer.

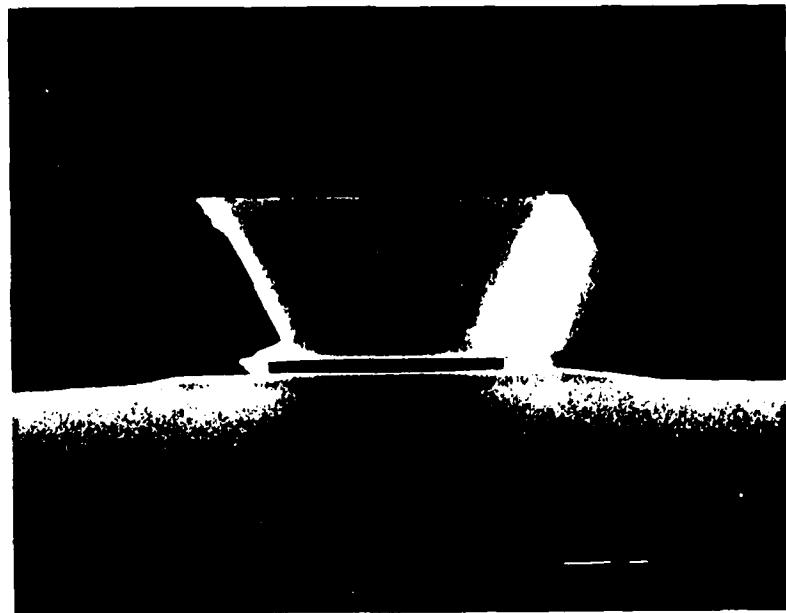


Figure 13A Reverse trapezoid structure before LPE.

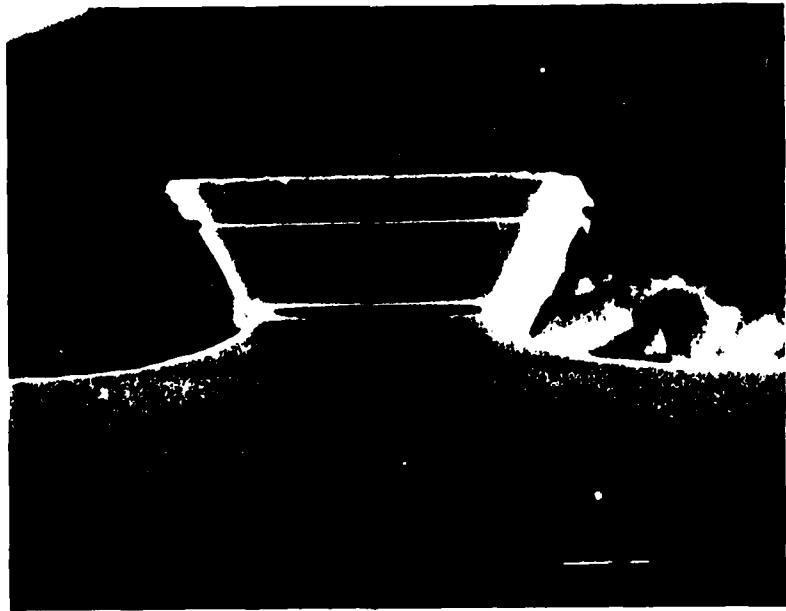
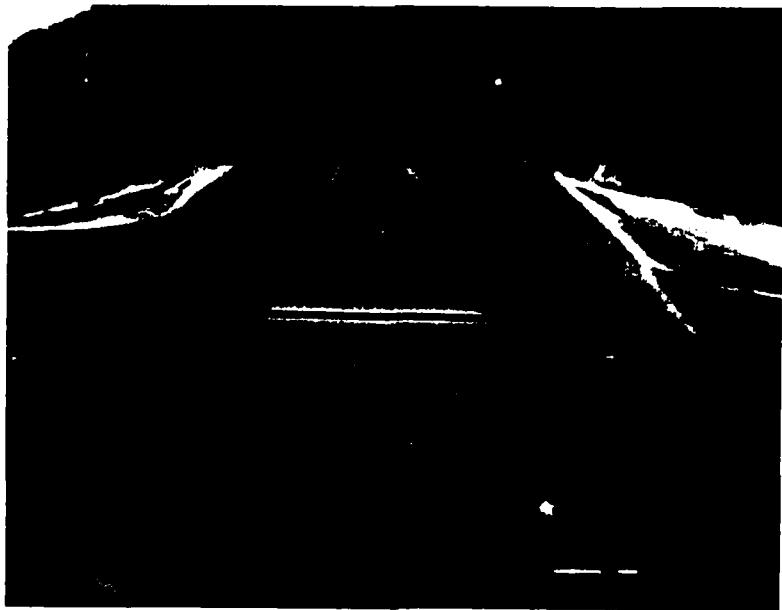


Figure 13B Reverse trapezoid structure before LPE.



**Figure 14A Shows figure 13a structure
after LPE, note melt-back.**



**Figure 14B Shows figure 13b structure
after LPE, note melt-back.**

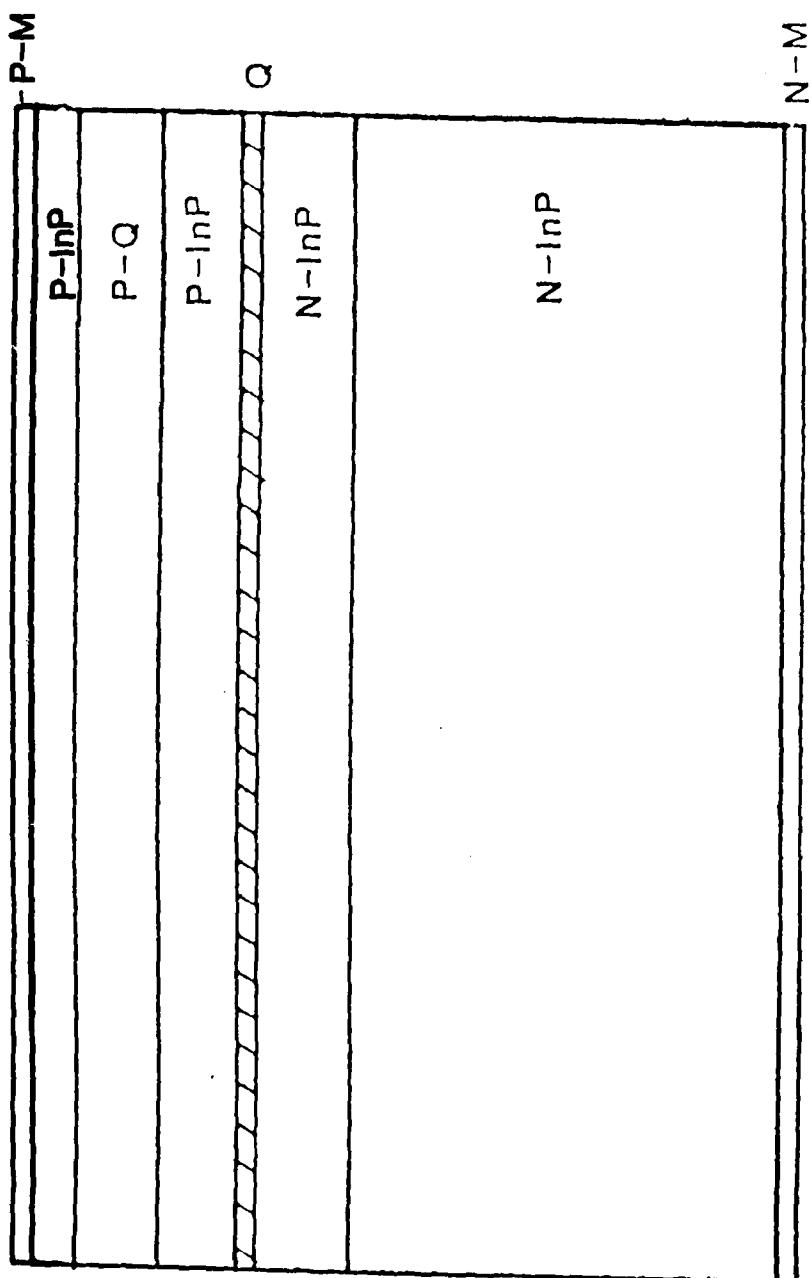
This was found not to be true by experimenting with the Si_3N_4 thickness. Thinning the Si_3N_4 layer has resulted in the Si_3N_4 breaking down which causes the complete melt back of the P-cap GaInAsP layer.

The excessive melt back which reduced the P-GaInAsP cap layer contact area resulted in many of the runs which yielded low pulsed threshold chips (I_{th} 80 to 150 mA) to have excessively high contact resistance which in turn resulted in premature burn-out occurring once the chips were mounted case positive and operated under CW condition. A typical device had forward voltages of 4 to 5 volts at threshold. Premature burn-out occurred at 5.5 volts.

5.0 MODIFIED (BH) BURIED HETEROJUNCTION LASER STRUCTURE

5.1 Structure and Technique

To resolve the extreme problems of melt back to the mesa structure during the regrowth of the N-P reverse bias junction, a new structure was introduced and is explained as follows: A five-layer (DH) double heterojunction structure is now being used and is shown in Figure 15. This structure consists of the following layers: (SN) doped InP substrate $N \sim 2 \times 10^{18} \text{ cm}^{-3}$ with (100) orientation with an etch pit density (EPD) of $< 7 \times 10^4 / \text{cm}^{-3}$; Sn doped N-InP cladding layer ($N \sim 1 \times 10^{17} \text{ cm}^{-3}$); undoped N-In_{0.708}Ga_{0.292}As_{0.0560}P_{0.440} quaternary active region ($N \sim 7.5 \times 10^{18} \text{ cm}^{-3}$); Zn doped InP cladding layer ($P \sim 1 \times 10^{18} \text{ cm}^{-3}$); a Zn doped P-In_{0.802}Ga_{0.198}As_{0.445}P_{0.455} quaternary cap layer ($P \sim 1 \times 10^{19} \text{ cm}^{-3}$); and an undoped P-InP cap layer. The layer thicknesses are 3.0, 0.2, 1.5, 0.7 and 0.5 μm respectively. The last layer, the Zn doped InP cap was the added modification to the standard (DH) double heterojunction structure which has been utilized since the start of the program. Melt compositions for this type structure are summarized in Figure 16. Scanning Electron microphotograph (S.E.M.), Figure 17 shows a stained cross section of the DH laser structure with an electron beam induced current (EBIC) trace, super imposed on the EPI layer micrograph. The (EBIC) trace



15 Five layer $GaInAsP/InP$ DH Structure

InP LPE RUN SHEET

Run #: QBH-186 Crystal #: InP434-R4 Furnace/boat: A1/RD3-A

Date: 9/15/9-16-80 Slice/Thickness: operator: D. L.

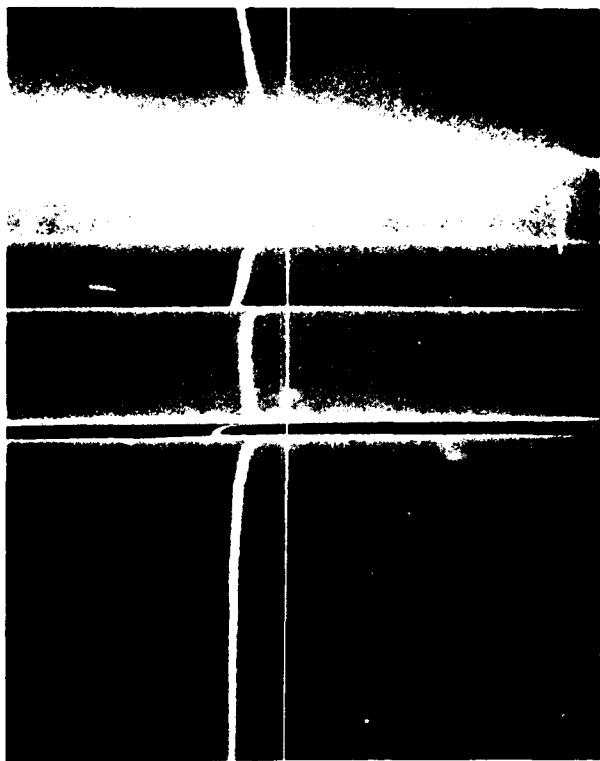
Run	In Ga	InP mm	InAs mm	GaAs mm	Dopants mm	Growth Period	Temp. °C	Layer Thickness
1	6	25.0	****	*****	*****	5 SEC.	636.0	
2	6	56.0	****	*****	399.0 (Sn)	5.0 °C	636.0	
3	6	69.0	400.0	95.0	*****	3 SEC.	631.0	
4	6	56.0	****	*****	5.0 (Zn)	2.0 °C	631.0	
5	6	39.0	302.0	38.0	1.0 (Zn)	1.0 °C	629.0	
6	6	56.0	****	*****	*****	0.8 °C	628.0	
						Thur	627.0	

Vacuum: A. 10 MTorr B. 10 MTorr A. 400cc Flow Rate: B. 400cc A. 45 Min. B. 25 Min. Flush Time: A. 180 Min. B. 60 Min. Saturate

Start: 644.5 °C Rate: 8 °C/hr. Grow: 636.0 °C

Notes: 5 layer structure with a double soak.
4 layer structure with a double soak.

Figure 16 Melt composition of five layer structure



**Figure 17 SEM and (EBIC) microphotographs of
five layer structure**

clearly shows the location of the P/N junction.

Figure 18 outlines the actual dimensions of the five layer GaInAsP/InP structure.

In conjunction with the added InP cap layer a double saturation technique was implemented.

As it is well known, the loss of phosphorus due to evaporation during the saturation periods can cause an increase in the etch rate of the etch melt. In the effort to control the rate of melt back 10 mgs. of InP was added to the etch melt to allow for the loss of P caused during saturation. Also a double saturation technique was implemented and this technique is explained as follows:

The multibin graphite slide boat is loaded with all the melt sources with the exception of InP sources. Zn dopants and the (BH) buried heterojunction structure processed from the five layer (DH) laser structure. The boat is then loaded into the reaction tube which is evacuated and flushed with purified hydrogen gas for one hour. The furnace is then rolled over the multibin boat and melts are then saturated for three hours at 635°C. Once the saturation period is completed the furnace is rolled back and the boat is allowed to cool to room temperature. The boat is then removed from the reaction tube and the InP sources

REQUISITION FOR SEM MICROGRAPH

Sample # RO-175B-H Date: 8/28/80

Structure:

Type of Micrograph Required: SE
AE/EBIC-LS Magnification
Thickness: SE 7-10KX

LAYER	LEFT	CENTER	RIGHT	AVERAGE
1. P-InP	1.0 μ	BH	1.0 μ	1.0 μ
2. N-InP	0.8 μ m	BH	0.9 μ m	0.85 μ m
3.				
4.				
5.				
6.				
7.				
8.				

Figure 18 SEM layer thickness outline

and Zn dopants are loaded into the respective bins, and the BH structure is loaded onto the graphite slider.

The boat is then re-loaded into the reaction tube where it is again evacuated, flushed and re-saturated at 635°C, this time for two hours. This two step saturation allows for a shorter time of saturation, allowing for a smaller loss of (P) during saturation.

5.2 RESULTS USING THE MODIFIED TECHNIQUE

Using this new five layer structure and new regrowth technique to aid in preventing melt back to the p-quaternary cap layer has resulted in successful growths such as seen in Figure 19. These S.E.M. microphotographs show the five-layer mesa structure before and after regrowth at a magnification of 7,000X. These microphotographs are representative of 10 LPE runs made using the mentioned technique. As it can be seen in these microphotographs, there is very little or no melt back to the p-quaternary layer which was seen in earlier attempts (Figure 14).

The reverse bias junction layer melt compositions are shown in Figure 20. In conjunction with optimizing the amount of melt back to the p-quaternary layer. The layer thicknesses were adjusted to allow for the even deposit of both N and P layers.



**Figure 19 SEM microphotographs of BH structure
before and after regrowth**

InP LPE RUN SHEET

Run # RQ-175 BH

Crystal # In P 434-R4

Furnace/Boat A1/RD3A

Date 8/25/80

Slice/Thickness BH Structure

Operator DL

in	In gm	InP mg	InAs mg	GaAs mg	Dopants mg	Growth Period	Temp. °C	Layer Thickness
1	6	35.0	xxxx	xxxx	xxxx	4 sec.	625°	
2	6	70.0	xxxx	xxxx	4.98 (Zn)	1.0 sec.	625°	
3	6	70.0	xxxx	xxxx	100.0 (Sn)	1.5 sec.	624°	
4						thru	622.5°	
5								
6								
7								
8								

Vacuum: A 15 mTorr B 10 mTorr Flow Rate: A 400cc B 400cc Flush Time: A 30 min. B 30 min. Saturate: A 60 min. B 60 min.

Start: _____ Rate: _____ Grow: _____

Comments:

Reverse bias junction re-growths with double saturation.

Figure 20 Melt composition of N-P reverse bias junction

These adjustments had to be made so that the area between the mesa structures would be filled without causing high shoulders on either side of the mesa structures, which in turn would cause high contact resistance.

These problems were resolved and this can be seen in Figure 19. Further optimization had to be done on the N-P reverse bias junction. All the runs made using the new five layer structure failed to produce (SLM) injection lasers due to the problem of current leakage into the reverse bias layer during CW operation. Typical test results from the new structure are as follows:

Pulsed threshold current $I_{th} = 80\text{mA}$ to 500mA , mounted data of diodes $I_{th} < 150\text{mA}$, Power (P_o) = $200-400\mu\text{W}$, forward voltage $V_f = 1.6-1.7$ Volt. Devices fabricated from these runs were examined more closely by using a metallurgy microscope in conjunction with an infrared scope. This enabled us to view the buried heterojunction structure while inducing current in the mounted devices. Using this technique, light could be seen emitting from the buried region, but it was noted that light was also seen emitting from the reverse bias N-P junction.

Figure 21 shows the buried heterojunction structure.

The arrows indicate these areas outside the active region which were also emitting light. Figure 22 shows the desired (BH) structure.

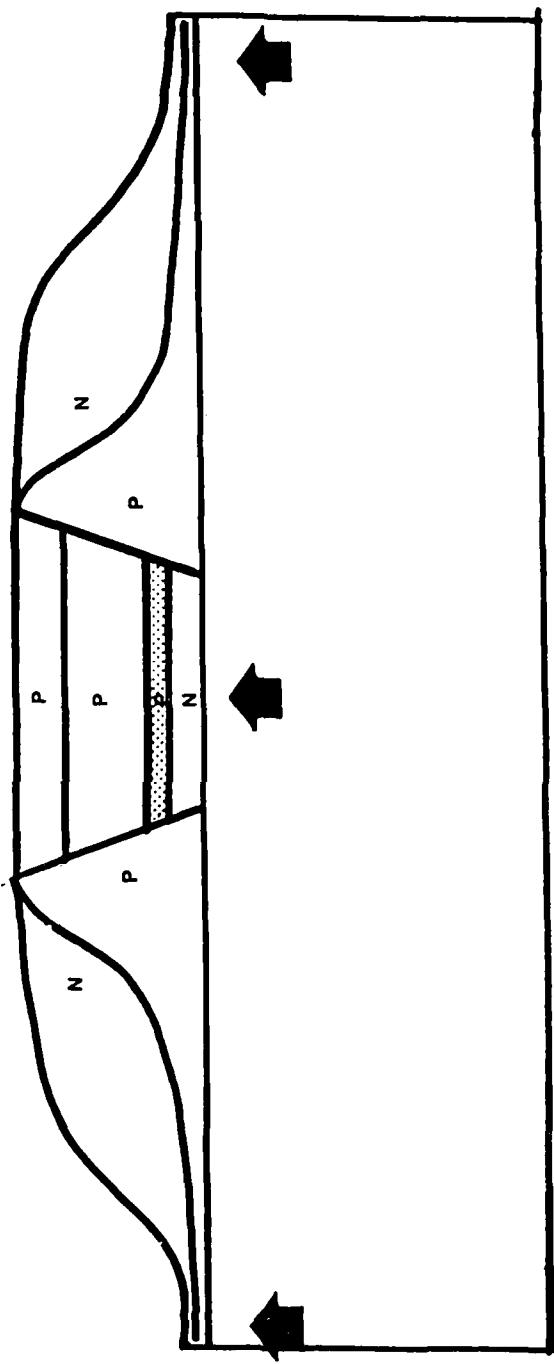
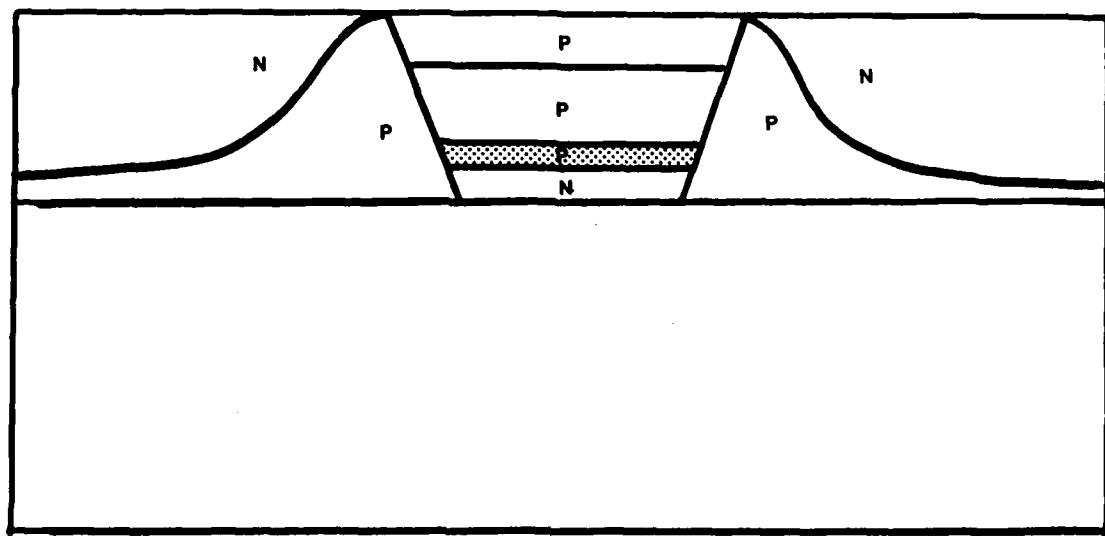


Figure 21 (BH) structure showing emitting areas outside the active region, current leakage



**Figure 22 (BH) structure showing normal regrowth
of N-P reverse bias junction**

6.0 PERFORMANCE CHARACTERISTICS

6.1 The histogram in Figure 23 shows a typical distribution of low threshold current, I_{th} chips yielded from the (BH) buried heterojunction laser structures using a pulsed threshold test procedure. All devices once mounted exhibited very poor efficiency, data as follows:

Typical Test Results $I_{th} = \infty$

$P_o = 400-600 \mu W$

$V_f = 1.6 - 1.7$ Volts

These test results were due to the reverse bias junction leakage, resulting in no current confinement to the active region as explained in Part 5.0.

6.2 Representative Devices Yield

The histogram in Figure 24 shows a typical distribution in pulsed threshold current, I_{th} , chip yield from the (DH) Double Hetero junction laser structure which was used in the attempt to develop a (BH) buried heterojunction laser structure. To monitor the structure carefully, every fifth (DH) structure was processed as a (DS) Diffused Stripe geometry laser structure. By doing this we were able to check in intervals to insure that such characteristics as I_{th} , λ , P_o were not effected by changes made in the structure during the program. As shown in the histogram, an exceptionally

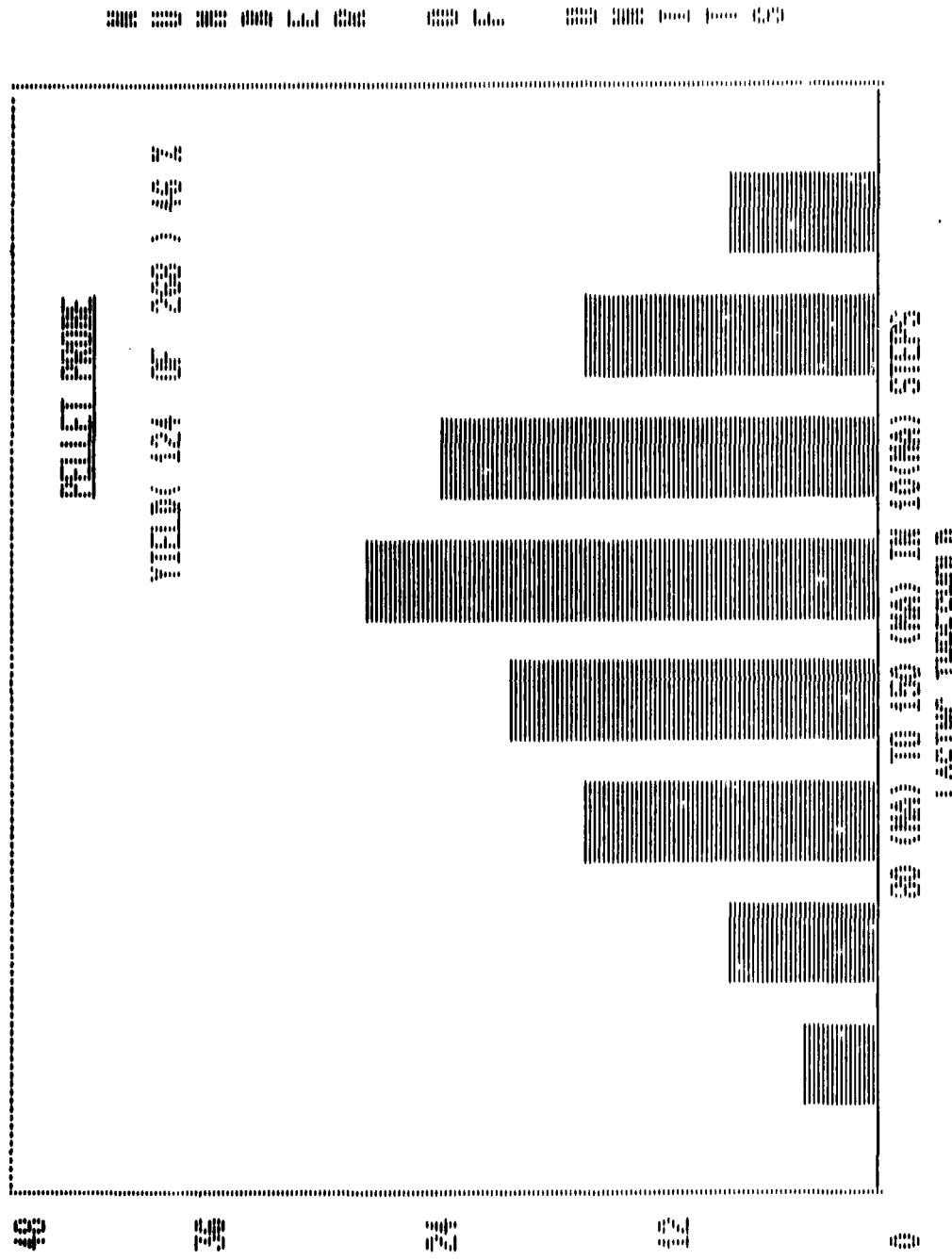


Figure 23 Bar diagram showing low pulsed threshold current chips yielded from (BH) structure

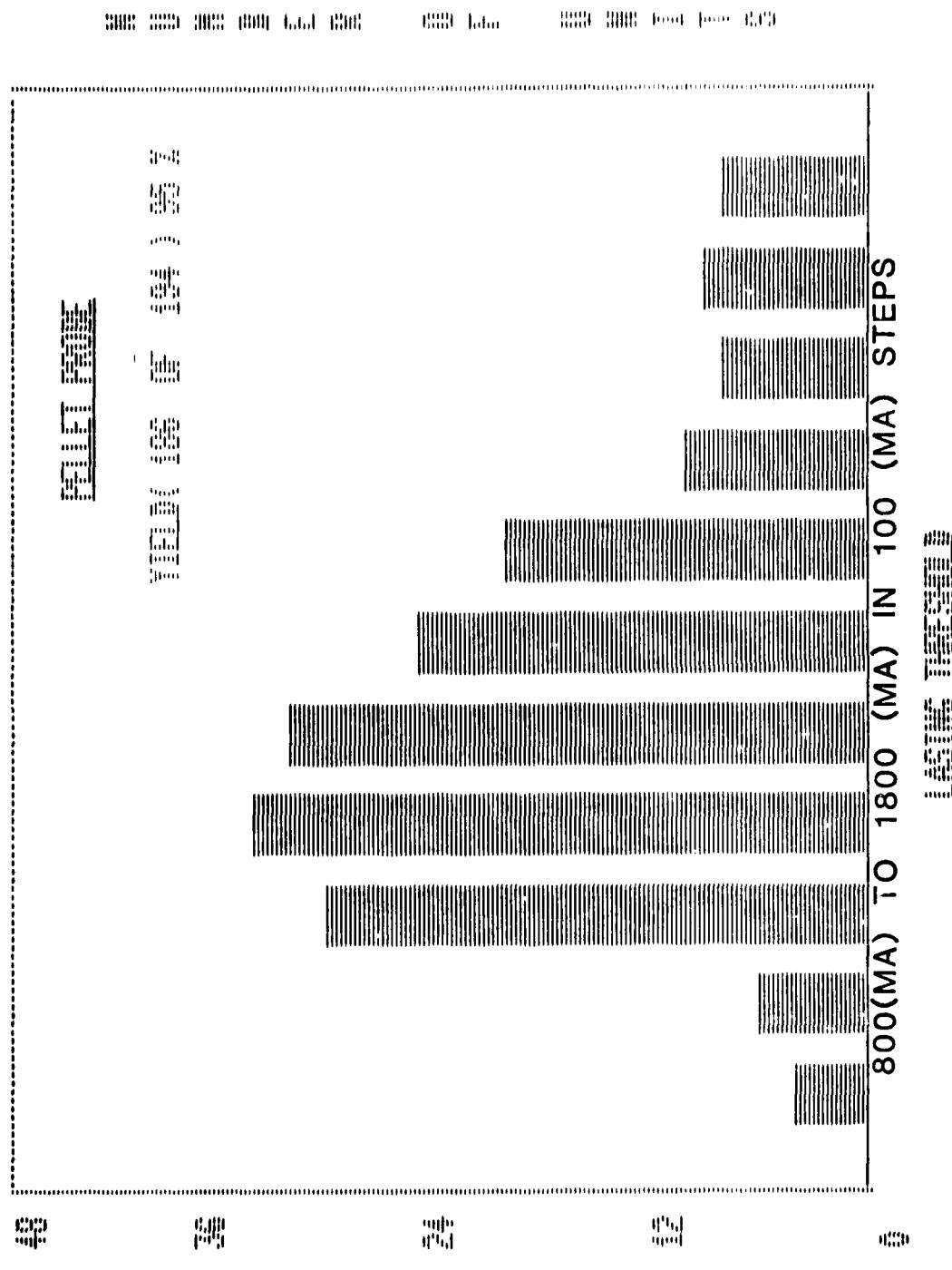


Figure 24 Bar diagram showing yield of pulsed threshold current chips yielded from (DH) structure

high yield was produced. Only 7% of the chips were non-lasers with the peak in the distribution around 1200 mA. Devices delivered under this contract were fabricated from chips having 800 to 1700 mA threshold. The average threshold current density assuming a diode area of 75 μm by 200 μm , is $16.5 \text{ A}/\text{cm}^2$ for the 0.2 μm wide cavity at $\lambda_p = 1.33 \mu\text{m}$. The $J_{th}/\mu\text{m}$ is roughly three times greater than for comparable GaAlAs ternary structures suggesting less effective carrier confinement in the quaternary.

Peak wavelength, threshold current, and total output power measurement at two times I_{th} are given in Figure 25 for devices delivered under this contract. Power output was measured at low duty factor (1KH_z , 50 NSEC) using a 1 millimeter diameter calibrated Ge pin photodiode (Rofin GE7460). The spectral responsibility curve for this diode is given in Figure 26. Calibration was accomplished using GaAs (904 μm) diodes of known power as determined with an NBS traceable ITT F4000 vacuum photodetector. These lasers had a far field distribution similar to that of the longwave quaternary lasers so that power collection was the same for both types. By measuring the GaAs diodes with the Ge detector and using the spectral responsivity curve, a calibration factor of 1.50 mW/mV at $\lambda_p = 1.35 \mu\text{m}$ was determined.

Diode #	I _{th} AMPS	I _m AMPS	P ₀ max mW	WAVELENGTH nm	TEST CONDITIONS:	
					Drive current=2xI _{th}	Frequency= 1kHz
1	1.3	2.6	138	1346		
3	1.7	3.4	129	1330		
4	0.9	1.8	138	1332		
5	0.8	1.6	120	1356		
6	3.3	6.6	294	1370		
7	1.0	2.0	120	1350		
8	0.8	1.6	120	1352		
11	1.1	2.2	138	1343		
15	0.9	1.8	147	1352		
16	0.9	1.8	129	1369		
17	1.0	2.0	138	1360		
18	0.7	1.4	110	1360		
19	0.9	1.8	74	1338		
21	0.9	1.8	92	1323		
22	0.8	1.6	138	1352		
25	1.0	2.0	129	1361		
26	0.8	1.6	129	1346		
29	1.5	3.0	129	1347		
31	1.5	3.0	83	1334		
35	1.5	3.0	74	1332		

Figure 25 Data sheet of devices delivered for contract, test conditions

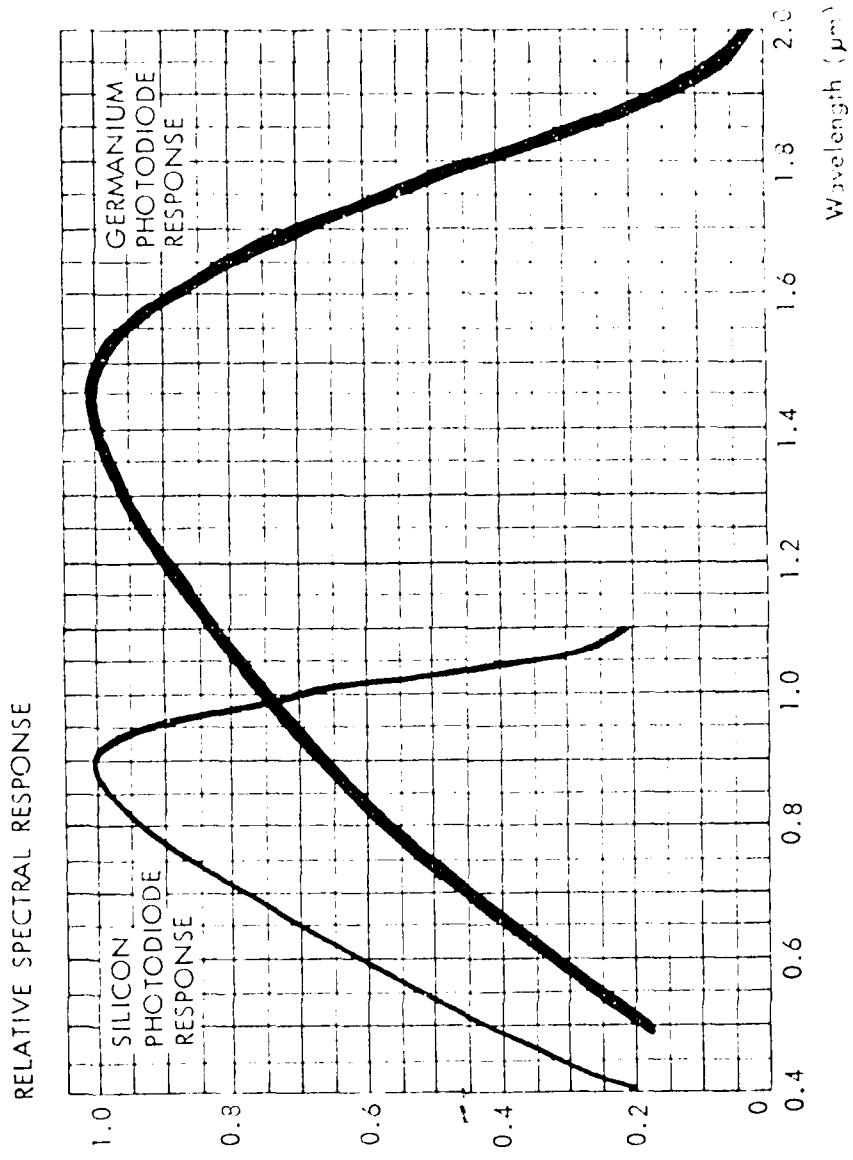


Figure 26 Spectral responsitivity curve for (GE) pin diode

Several hundred milliwatts total output was reliably achieved and the average differential efficiency (DQE) was 0.20 mW/mA per facet for the 20 lasers delivered without fibers. Although the delivered diodes were conservatively rated at only $2.0 \times I_{th}$ or slightly greater than $4 \text{ mW}/\mu\text{m}$ of active junction length, about twice this power level can be achieved before one begins to observe the onset of catastrophic damage.

Figure 27 shows a typical output spectrum from the quaternary LOC with the output peak located at $1.35 \mu\text{m}$ and the spectral half width of 2 nm.

Figure 28 and 29 show the parallel and perpendicular far field beam divergence typically observed for these devices, respectively. The parallel equals 17° and perpendicular equals 35° FWHW divergence indicating a fairly high degree of optical confinement for the $0.20 \mu\text{m}$ cavity width device. This can be reduced by making the active region much wider but with a severe penalty in threshold current.

Improved performance for fiber coupled devices could be achieved by further reduction of the stripe width accompanied by a corresponding increase in active region thickness. This would provide a more suitable

Figure 27 Typical lasing spectral scan for pulsed device delivered under the contract.

RQ-197

Drive current 1.6A

Pulse width 50 n.sec.

Frequency 1KHz

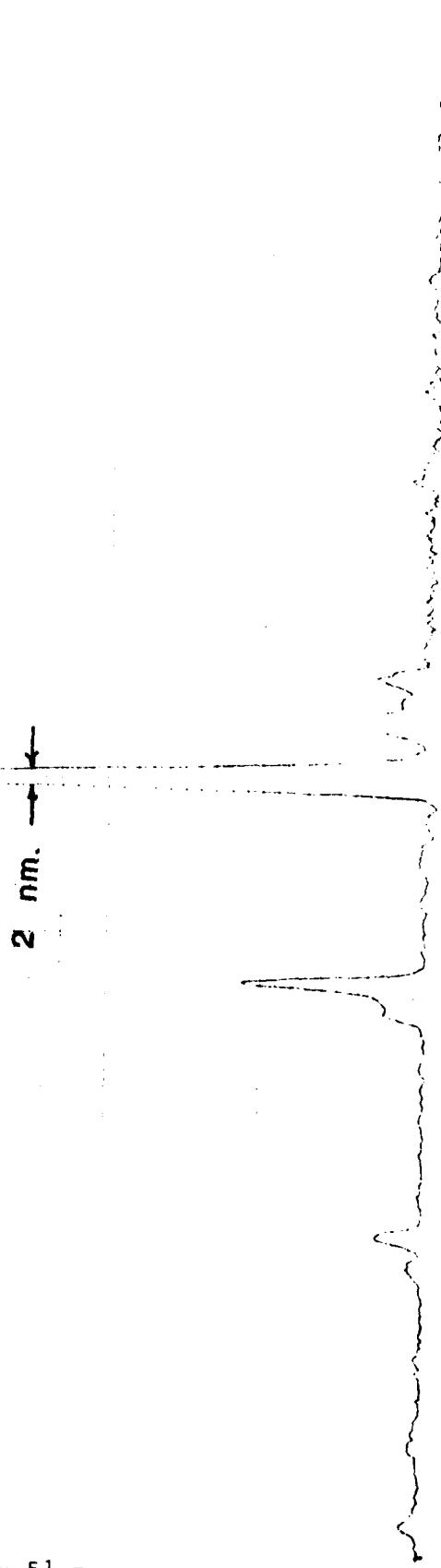


Figure 28 Parallel beam divergence for pulsed devices delivered under the control of

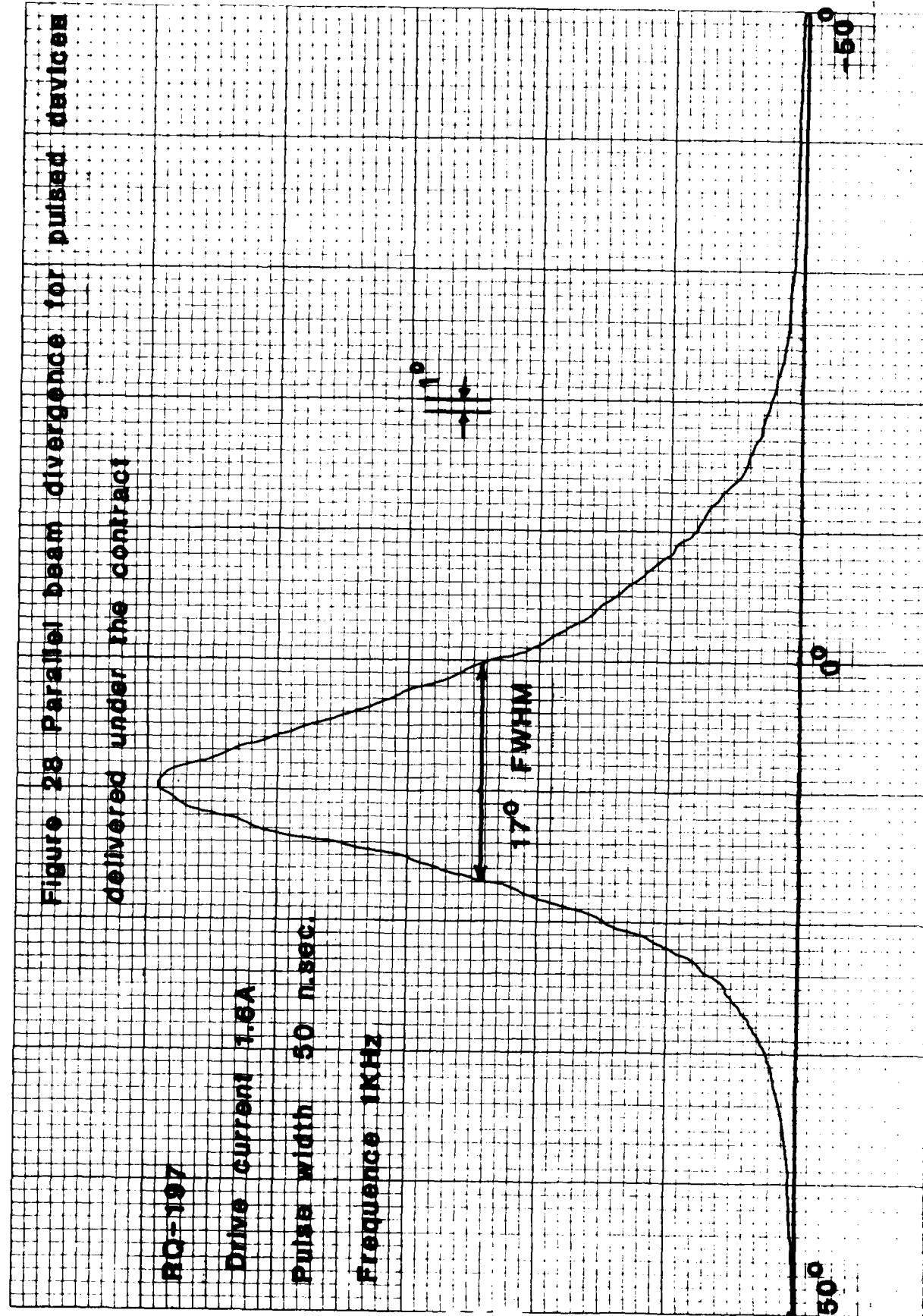
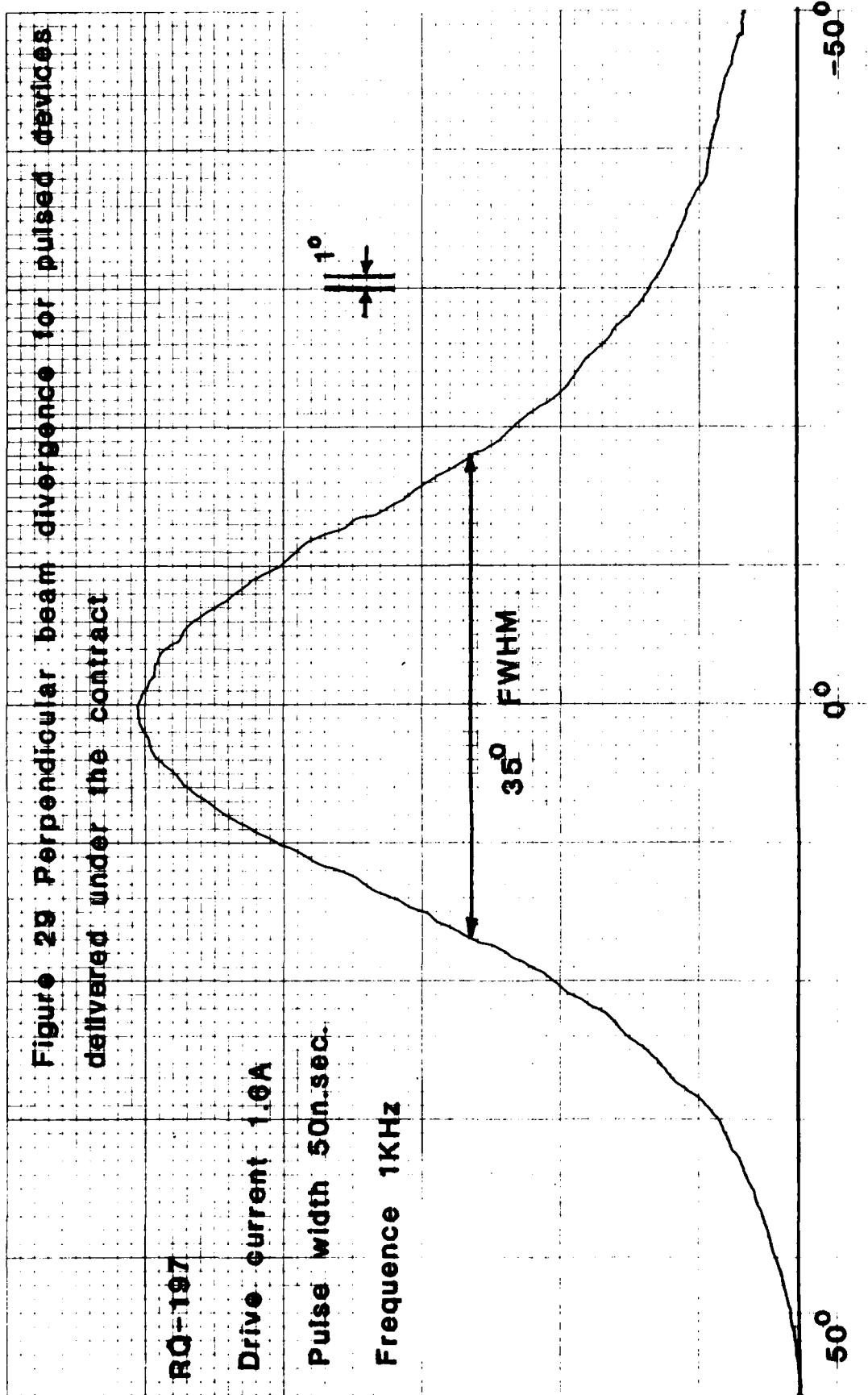


Figure 29 Perpendicular beam divergence for pulsed devices
delivered under the contract



match to 50 μm core fibers and reduce the beam divergence. The threshold and DQE for such devices would be approximately the same as the course of this program.

7.1 SUMMARY AND CONCLUSION

During the extent of the contract to develop long wavelength (λ -1.3 μm) single mode (SLM) injection laser diodes, utilizing a buried heterojunction (BH) laser structure, many noteworthy advances were accomplished and are as follows:

A multilayer quaternary liquid phase epitaxial growth technique was developed resulting in excellent layer uniformity and thickness control as well as surface morphology. In the course of developing a quaternary growth technique, a wavelength dopant technique was acquired in which wavelength became more predictable and could be controlled accurately from run to run. This technique was acquired using reference #12, IEEE Journal of Quantum Electronics, Vol. QE-16 #2 Feb. 1980 by Yoshio Itaya, Shigehisa Arai and Yasuharu Suematsu.

The most impressive accomplishment made during the contract was the regrowth technique developed in which the reverse trapezoid mesa is buried using a reverse bias N-P junction. This is explained in Section 5.0, Page 32 thru 40. This technique was very successful in aiding in the regrowth technique so that the amount of melt back was reduced and is shown in microphotographs in Figure 19.

As the contract stands the main problem hampering the successful completion, is the optimization of the reverse bias (N-P) junction. As reported the need to optimize and control these layer thicknesses is extremely critical to successfully confining the buried heterojunction mesa structure for both optical confinement and threshold reduction. The problem with the technique now being used is device efficiency was reduced due to current leakage which is due to poor confinement characteristics of the N-P reverse bias junction. The two main problems that are the cause of the current leakage are, the dopant characteristics of the N-P junction, and the other is the LPE regrowth layer thickness control. Figure 21 and 22 shows the difference between what we presently have and what is needed to give the current and optical confinement.

The final goals would be to work on the second regrowth technique and to adjust the dopant of the reverse bias junction in order to successfully confine the buried mesa structure. Considering the yield of devices under pulsed test operation, with thresholds of 80 to 150 mA and a typical power output of these devices was 200-500 μ W under CW operation. With more work the success of this project would be very promising once the problems explained herein were resolved.

The devices sent to fill the contract order are typical of those devices yielded from the (DH) Double Heterojunction structure used in the development of the (BH) laser structure.

The (DH) structure is explained in the final report. Stripe geometries were formed using a Si_3N_4 blocking layer, stripe widths were 10 μm . Chip yield was very high (avg. 89%), pulsed threshold currents ranged from 800 mA to 2000 mA. All measurements were done using a low duty factor of (1K Hz , 50nsec) at two times I_{th} . Test results are as follows: $I_{th} = 1.15\text{A}$ $I_m = 2.3\text{A}$ $P_o \text{ Max} = 128\text{mW}$ wavelength = 1.35 μm .

A typical output spectrum from these devices is shown

in the final report and shows a 2 nm spectral half width. Far field beam divergence typically observed for these devices were 17° and 35° for parallel and perpendicular, respectively. These results show a very high degree optical confinement in the transverse directions.

As demonstrated, transverse mode control can be achieved by using the DH structure and narrow stripe geometry, operating under pulsed current conditions. With more work on the buried heterojunction (BH) structure, single longitudinal mode (SLM) injection lasers can be demonstrated in the future.

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